



General Description

- 100% UIS Tested
- Advanced Trench Technology
- Low Gate Charge
- High Current Capability
- RoHS and Halogen-Free Compliant

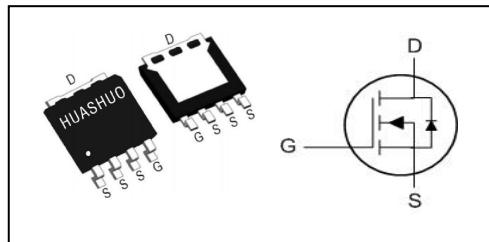
Product Summary

V_{DS}	40	V
$R_{DS(ON),TYP}$	0.5	$m\Omega$
I_D	330	A

Applications

- SMPS Synchronous Rectification
- DC/DC Converters
- Or-ing

LFPAK5X6 Pin Configuration



Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	40	V
V_{GS}	Gate-Source Voltage	± 20	V
$I_D@T_c=25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V^{1,6}$	330	A
$I_D@T_c=100^\circ C$	Continuous Drain Current, $V_{GS} @ 10V^{1,6}$	200	A
$I_D@T_A=25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V^1$	45	A
$I_D@T_A=100^\circ C$	Continuous Drain Current, $V_{GS} @ 10V^1$	35	A
I_{DM}	Pulsed Drain Current ²	530	A
EAS	Single Pulse Avalanche Energy ³	580	mJ
I_{AS}	Avalanche Current	106	A
$P_D@T_c=25^\circ C$	Total Power Dissipation ⁴	140	W
$P_D@T_A=25^\circ C$	Total Power Dissipation ⁴	2.5	W
T_{STG}	Storage Temperature Range	-55 to 150	$^\circ C$
T_J	Operating Junction Temperature Range	-55 to 150	$^\circ C$

Thermal Data

Symbol	Parameter	Typ.	Max.	Unit
$R_{\theta JA}$	Thermal Resistance Junction-Ambient ¹	---	50	$^\circ C/W$
$R_{\theta JC}$	Thermal Resistance Junction-Case ¹	---	0.9	$^\circ C/W$



Electrical Characteristics ($T_J=25^\circ\text{C}$, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{\text{GS}}=0\text{V}$, $I_D=250\mu\text{A}$	40	---	---	V
$R_{\text{DS}(\text{ON})}$	Static Drain-Source On-Resistance ²	$V_{\text{GS}}=10\text{V}$, $I_D=20\text{A}$	---	0.5	0.9	$\text{m}\Omega$
		$V_{\text{GS}}=4.5\text{V}$, $I_D=20\text{A}$	---	0.85	1.2	
$V_{\text{GS}(\text{th})}$	Gate Threshold Voltage	$V_{\text{GS}}=V_{\text{DS}}$, $I_D=250\mu\text{A}$	1.2	1.7	2.2	V
I_{DSS}	Drain-Source Leakage Current	$V_{\text{DS}}=32\text{V}$, $V_{\text{GS}}=0\text{V}$, $T_J=25^\circ\text{C}$	---	---	1	uA
		$V_{\text{DS}}=32\text{V}$, $V_{\text{GS}}=0\text{V}$, $T_J=55^\circ\text{C}$	---	---	5	
I_{GSS}	Gate-Source Leakage Current	$V_{\text{GS}}=\pm 20\text{V}$, $V_{\text{DS}}=0\text{V}$	---	---	± 100	nA
R_g	Gate Resistance	$V_{\text{DS}}=0\text{V}$, $V_{\text{GS}}=0\text{V}$, $f=1\text{MHz}$	---	1.3	---	Ω
Q_g	Total Gate Charge (10V)	$V_{\text{DS}}=20\text{V}$, $V_{\text{GS}}=10\text{V}$, $I_D=20\text{A}$	---	128	---	nC
Q_g	Total Gate Charge (4.5V)		---	67	---	
Q_{gs}	Gate-Source Charge		---	17	---	
Q_{gd}	Gate-Drain Charge		---	29	---	
$T_{\text{d}(\text{on})}$	Turn-On Delay Time	$V_{\text{DD}}=20\text{V}$, $V_{\text{GS}}=10\text{V}$, $R_G=1.5\Omega$, $I_D=20\text{A}$	---	22	---	ns
T_r	Rise Time		---	149	---	
$T_{\text{d}(\text{off})}$	Turn-Off Delay Time		---	55	---	
T_f	Fall Time		---	17	---	
C_{iss}	Input Capacitance	$V_{\text{DS}}=20\text{V}$, $V_{\text{GS}}=0\text{V}$, $f=1\text{MHz}$	---	6810	---	pF
C_{oss}	Output Capacitance		---	2119	---	
C_{rss}	Reverse Transfer Capacitance		---	222	---	

Diode Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_s	Continuous Source Current ^{1,6}	$V_G=V_D=0\text{V}$, Force Current	---	---	100	A
V_{SD}	Diode Forward Voltage ²	$V_{\text{GS}}=0\text{V}$, $I_s=1\text{A}$, $T_J=25^\circ\text{C}$	---	---	1.2	V
T_{rr}	Reverse Recovery Time	$I_f=20\text{A}$, $dI/dt=100\text{A}/\mu\text{s}$,	---	77	---	nS
Q_{rr}	Reverse Recovery Charge	$T_J=25^\circ\text{C}$	---	91	---	nC

Note :

- 1.The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper.
- 2.The data tested by pulsed , pulse width $\leq 300\mu\text{s}$, duty cycle $\leq 2\%$
- 3.The EAS data shows Max. rating . The test condition is $V_{\text{DD}}=25\text{V}$, $V_{\text{GS}}=10\text{V}$, $L=0.1\text{mH}$, $I_{\text{AS}}=106\text{A}$
- 4.The power dissipation is limited by 150°C junction temperature
- 5.The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.
- 6.Package limitation current is 100A.



Typical Characteristics

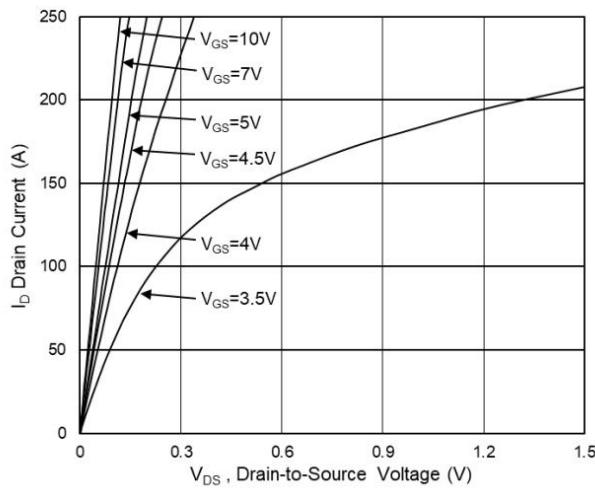


Fig.1 Typical Output Characteristics

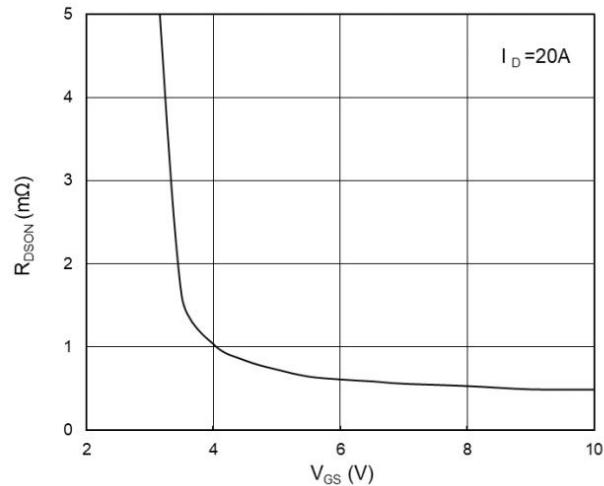


Fig.2 On-Resistance vs G-S Voltage

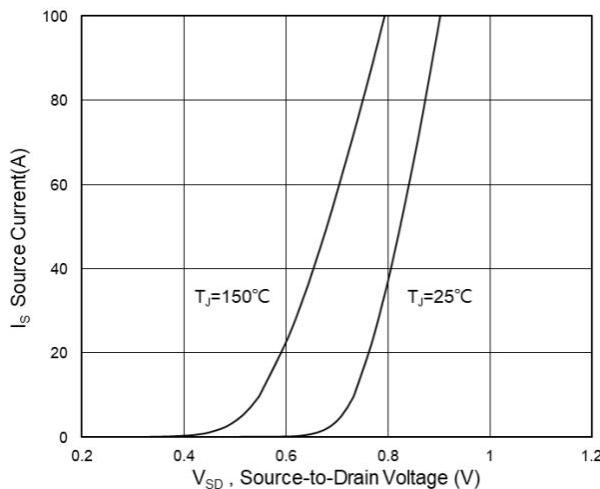


Fig.3 Source Drain Forward Characteristics

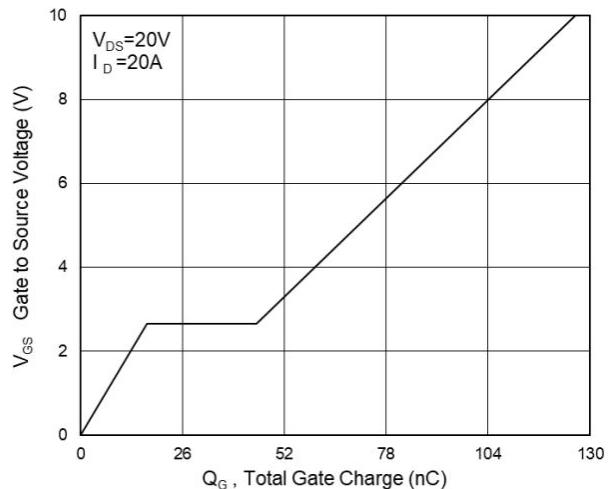


Fig.4 Gate-Charge Characteristics

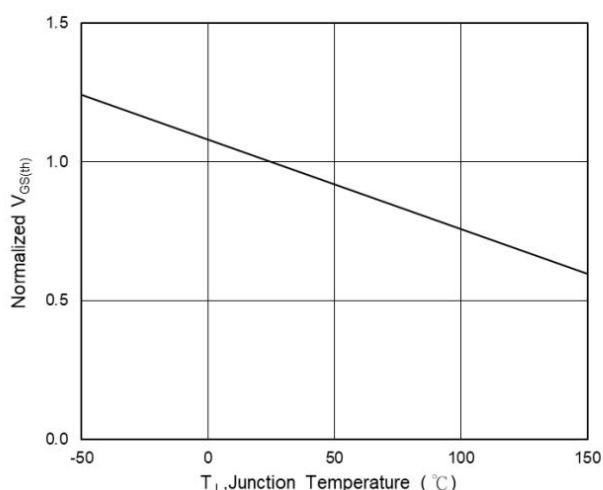


Fig.5 Normalized $V_{GS(th)}$ vs T_J

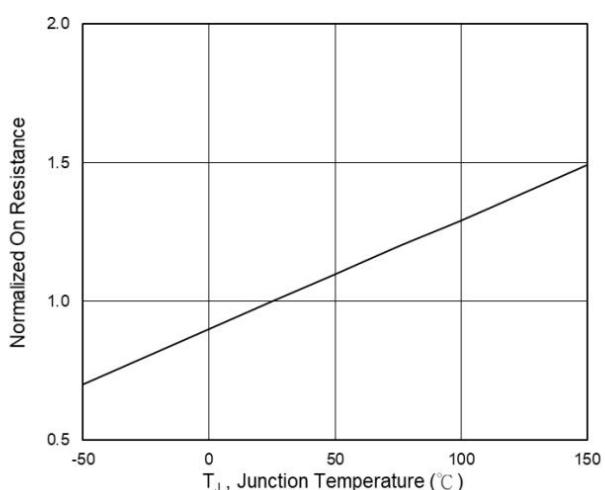


Fig.6 Normalized $R_{DS(on)}$ vs T_J



N-Ch 40V Fast Switching MOSFETs

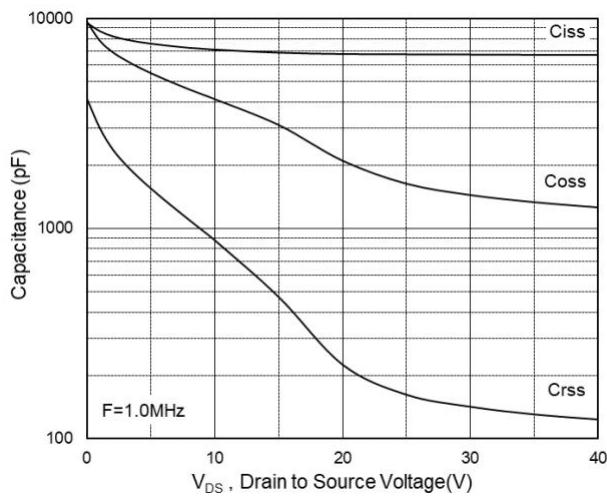


Fig.7 Capacitance

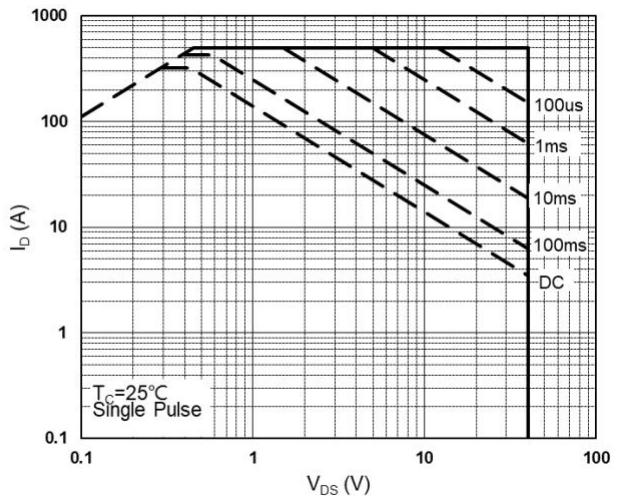


Fig.8 Safe Operating Area

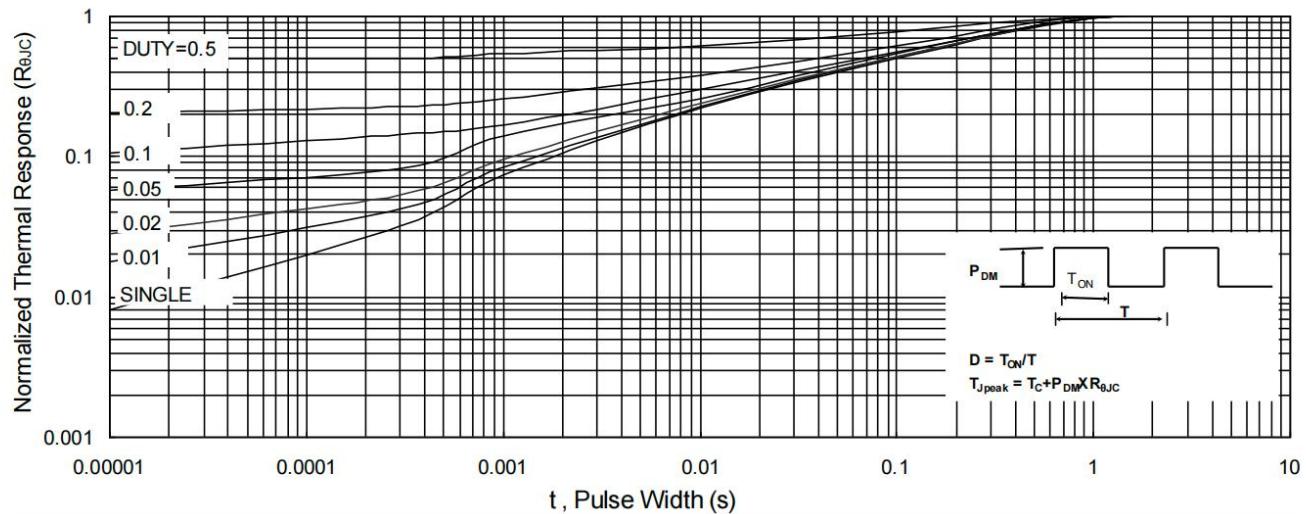


Fig.9 Normalized Maximum Transient Thermal Impedance

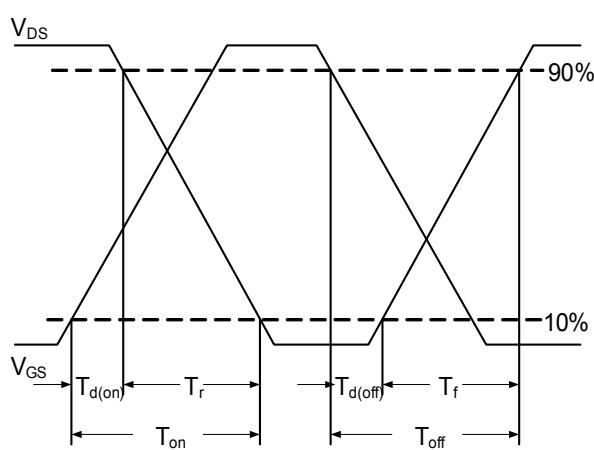


Fig.10 Switching Time Waveform

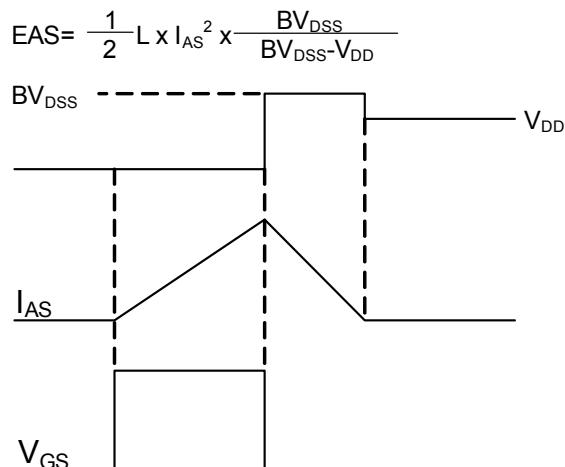


Fig.11 Unclamped Inductive Switching